What is claimed is:

1. A semiconductor test apparatus comprising:

an input data generating unit that generates the measured data applied to the test device based on the input measurement conditions;

an expected data generating unit that generates expected data based on said measurement conditions;

a determination unit that compares the measurement result data that said test device outputs to the expected data based on said measurement data, determines whether the function of said device is a pass or failure, and outputs the determination result data as the determination result; and

a data log system unit that writes into the log memory in a time sequence the associated data that includes said determination result data, measurement result data, measurement expectation data, and measurement input data; wherein

said data log system unit writes this associated data into the log memory for a predetermined period even after any of said associated data or the address of the log memory satisfy the preset write termination conditions that terminate the writing.

2. A semiconductor test apparatus according to claim 1 wherein said data log system continues to write said associated data into the log memory over an extended time range indicated by input write extension conditions even after the write termination conditions have been satisfied.

3. A semiconductor test apparatus according to claim 1 wherein said data log system writes said associated data into a predetermined address of the log memory at each time

unit in which a determination about the pass or failure of the test device is made.

4. A semiconductor test apparatus according to claim 1 wherein said log memory has a predetermined address range, and is structured so as to overwrite the subsequent associated data from the head address after writing the associated data in the final address.

5. A semiconductor test apparatus according to claim 1 wherein said data log system increments the address of said log memory at each time unit that a determination of the pass or failure of the test device is made, and writes in sequence said associated data.